# GaNFast™ Power IC



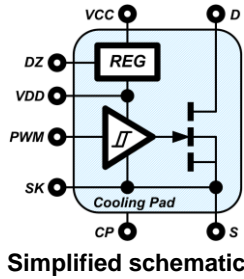**QFN 6 x 8 mm**



**Simplified schematic**

## 2. Description

The NV6128 is a thermally-enhanced version of the popular GaNFast™ power IC, optimized for high frequency and soft-switching topologies.

Monolithic integration of FET, drive and logic creates an easy-to-use 'digital-in, power-out' high-performance powertrain building block, enabling designers to create the fastest, smallest, most efficient integrated powertrain in the world.

The highest dV/dt immunity, high-speed integrated drive and industry-standard low-profile, low-inductance, 6 x 8 mm SMT QFN package allow designers to exploit Navitas GaN technology with simple, quick, dependable solutions for breakthrough power density and efficiency.

Navitas' GaNFast™ power ICs extend the capabilities of traditional topologies such as flyback, half-bridge, resonant, etc. to MHz+ and enable the commercial introduction of breakthrough designs.

## 1. Features

### GaNFast™ Power IC

- Large cooling pad
- Enhanced thermals when using CS resistor
- Monolithically-integrated gate drive
- Wide $V_{CC}$ range (10 to 30 V)
- Programmable turn-on dV/dt
- Source Kelvin ground
- 200 V/ns dV/dt immunity

- Low 70 mΩ resistance

- 800V transient voltage rating
- 650V continuous voltage rating
- 2 kV ESD rating (HBM)
- Zero reverse recovery charge
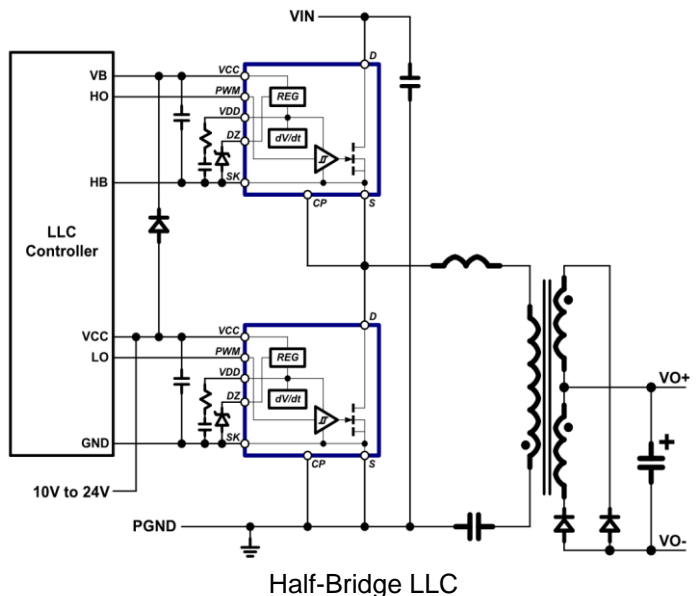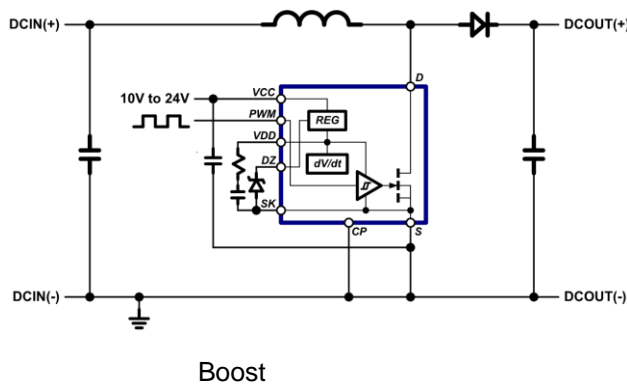- 2 MHz operation

### Small, low-profile SMT QFN

- 6 x 8 mm footprint, 0.85 mm profile
- Minimized package inductance

### Environmental

- RoHS, Pb-free, REACH-compliant

## 3. Topologies / Applications

- AC-DC, DC-DC, DC-AC
- Buck, boost, half bridge, full bridge
- Active Clamp Flyback, LLC resonant, Class D
- Quasi-Resonant Flyback
- Mobile fast-chargers, adapters
- Notebook adaptors
- LED lighting, solar micro-inverters
- TV / monitor, wireless power
- Server, telecom & networking SMPS

## 4. Typical Application Circuits



Boost



Half-Bridge LLC

## 5. Table of Contents

# 6. Specifications

## 6.1. Absolute Maximum Ratings[1]

(with respect to Source (pad) unless noted)

| SYMBOL | PARAMETER | MAX | UNITS |
|---|---|---|---|
| $V_{DS}$ (TRAN) | Transient Drain-to-Source Voltage[2] | 800 | V |
| $V_{DS}$ (CONT) | Continuous Drain-to-Source Voltage | -7 to +650 | V |
| $V_{CC}$ | Supply Voltage | 30 | V |
| $V_{PWM}$ | PWM Input Pin Voltage | -3 to +30 | V |
| $V_{DZ}$ | $V_{DD}$ Setting Pin Voltage | 6.6 | V |
| $V_{DD}$ | Drive Supply Voltage | 7.5 | V |
| $V_{CP}$ | Cooling Pad Voltage | -10 to +10 | V |
| $I_D$ | Continuous Drain Current (@ $T_C$ = 100ºC) | 20 | A |
| $I_D$ PULSE | Pulsed Drain Current (10 µs @ $T_J$ = 25ºC) | 40 | A |
| $I_D$ PULSE | Pulsed Drain Current (10 µs @ $T_J$ = 125ºC) | 25 | A |
| dV/dt | Slew Rate on Drain-to-Source | 200 | V/ns |
| $T_J$ | Operating Junction Temperature | -55 to 150 | ºC |
| $T_{STOR}$ | Storage Temperature | -55 to 150 | ºC |

*(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.*

*(2) $V_{DS (TRAN)}$ allows for surge ratings during non-repetitive events that are < 100 µs (for example start-up, line interruption) and repetitive events that are < 100 ns (for example repetitive leakage inductance spikes). Refer to Section 8.9 for detailed recommended design guidelines.*

## 6.2. Recommended Operating Conditions[3]

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{DZ}$ | Drive Supply Set Zener Voltage[4] | 5.8 | 6.2 | 6.6 | V |
| $I_{DD\_EXT}$ | Regulator External Load Current | | | 3.0 | mA |
| $R_{DD}$ | Gate Drive Turn-On Current Set Resistance[5] | 10 | 25 | | Ω |
| $V_{PWM}$ | PWM Input Pin Voltage | 0 | 5 | Min. of ($V_{CC}$ or 20) | V |
| $V_{CC}$ | Supply Voltage | 10 | | 24 | V |
| $T_C$ | Operating Case Temperature | -40 | | 125 | ºC |

*(3) Exposure to conditions beyond maximum recommended operating conditions for extended periods of time may affect device reliability.*

*(4) Use of Zener diode other than 6.2 V is not recommended. See Table I for recommended part numbers of 6.2 V Zener diodes.*

*(5) $R_{DD}$ resistor must be used. Minimum 10 Ohm to ensure application and device robustness.*

## 6.3. ESD Ratings

| SYMBOL | PARAMETER | MAX | UNITS |
|--------|-----------|-----|-------|
| HBM | Human Body Model (per JS-001-2014) | 2,000 | V |
| CDM | Charged Device Model (per JS-002-2014) | 1,000 | V |

## 6.4. Thermal Resistance

| SYMBOL | PARAMETER | TYP | UNITS |
|--------|-----------|-----|-------|
| $R_{\theta JC}$ [6] | Junction-to-Case | 1.2 | ºC/W |
| $R_{\theta JA}$ [6] | Junction-to-Ambient | 40 | ºC/W |

*(6) $R_\theta$ measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)*

## 6.5. Electrical Characteristics

Typical conditions: $V_{DS}$ = 400 V, $V_{CC}$ = 15 V, $V_{DZ}$ = 6.2 V, $F_{SW}$ = 1 MHz, $T_{AMB}$ = 25 ºC, $I_D$ = 10 A, $R_{DD}$ = 10 Ω (or specified)

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| | **$V_{CC}$ Supply Characteristics** | | | | | |
| $I_{QCC}$ | $V_{CC}$ Quiescent Current | | 0.85 | 2 | mA | $V_{PWM}$ = 0 V |
| $I_{QCC-SW}$ | $V_{CC}$ Operating Current | | 4.5 | | mA | $F_{SW}$ = 1 MHz, $V_{DS}$ = Open |
| | **Low-Side Logic Input Characteristics** | | | | | |
| $V_{PWMH}$ | Input Logic High Threshold (rising edge) | | | 4 | V | |
| $V_{PWML}$ | Input Logic Low Threshold (falling edge) | 1 | | | V | |
| $V_{I-HYS}$ | Input Logic Hysteresis | | 0.5 | | V | |
| $T_{ON}$ | Turn-on Propagation Delay | | 15 | | ns | Fig.1, Fig.2 |
| $T_{OFF}$ | Turn-off Propagation Delay | | 15 | | ns | Fig.1, Fig.2 |
| $T_R$ | Drain rise time | | 10 | | ns | Fig.1, Fig.2 |
| $T_F$ | Drain fall time | | 5 | | ns | Fig.1, Fig.2 |
| | **Switching Characteristics** | | | | | |
| $F_{SW}$ | Switching Frequency | | | 2 | MHz | |
| $t_{PW}$ | Pulse width | 0.02 | | 1000 | µs | |
| | **GaN FET Characteristics** | | | | | |
| $I_{DSS}$ | Drain-Source Leakage Current | | 0.75 | 25 | µA | $V_{DS}$ = 650 V, $V_{PWM}$ = 0 V |
| $I_{DSS}$ | Drain-Source Leakage Current | | 20 | 50 | µA | $V_{DS}$ = 650 V, $V_{PWM}$ = 0 V, $T_C$ = 125 ºC |
| $R_{DS(ON)}$ | Drain-Source Resistance | | 70 | 100 | mΩ | $V_{PWM}$ = 6 V, $I_D$ = 10 A |
| $R_{DS(ON)}$ | Drain-Source Resistance | | 145 | | mΩ | $V_{PWM}$ = 6 V, $I_D$ = 10 A, $T_C$ = 125 ºC |
| $V_{SD}$ | Source-Drain Reverse Voltage | | 3.2 | 5 | V | $V_{PWM}$ = 0 V, $I_{SD}$ = 10 A |
| $Q_{OSS}$ | Output Charge | | 48 | | nC | $V_{DS}$ = 400 V, $V_{PWM}$ = 0 V |
| $Q_{RR}$ | Reverse Recovery Charge | | 0 | | nC | |
| $C_{OSS}$ | Output Capacitance | | 47 | | pF | $V_{DS}$ = 400 V, $V_{PWM}$ = 0 V |
| $C_{O(er)}$ [7] | Effective Output Capacitance, Energy Related | | 72 | | pF | $V_{DS}$ = 400 V, $V_{PWM}$ = 0 V |
| $C_{O(tr)}$ [8] | Effective Output Capacitance, Time Related | | 120 | | pF | $V_{DS}$ = 400 V, $V_{PWM}$ = 0 V |

*(7) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 400 V*

*(8) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 400 V*

## 6.6. Switching Waveforms
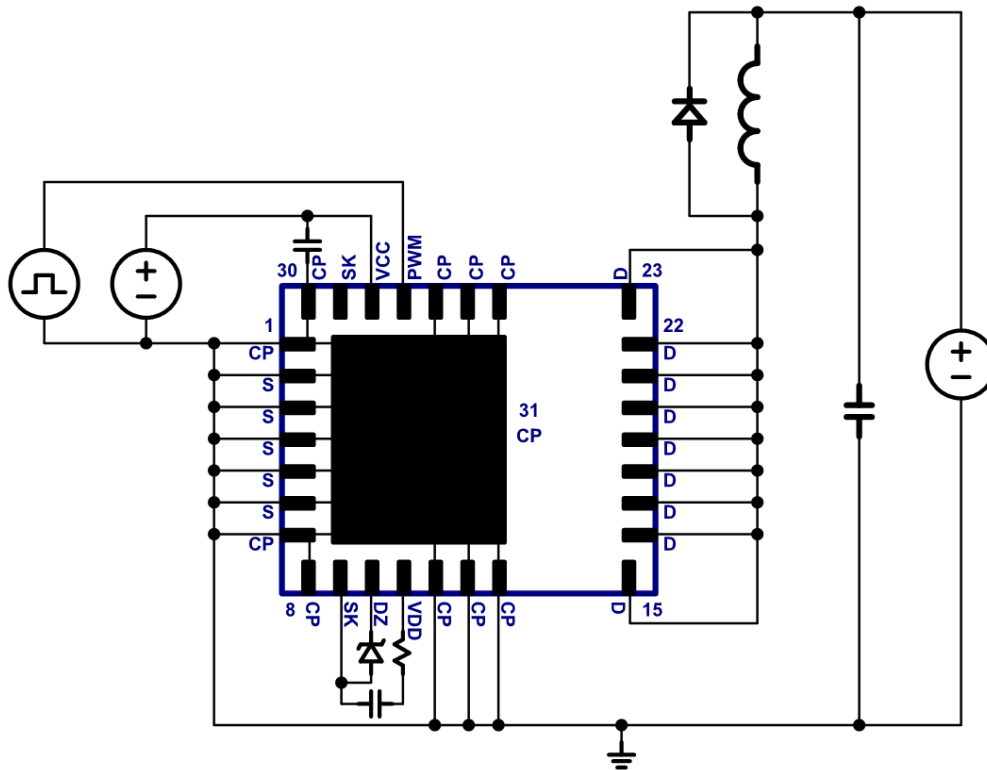
($T_C$ = 25 ºC unless otherwise specified)
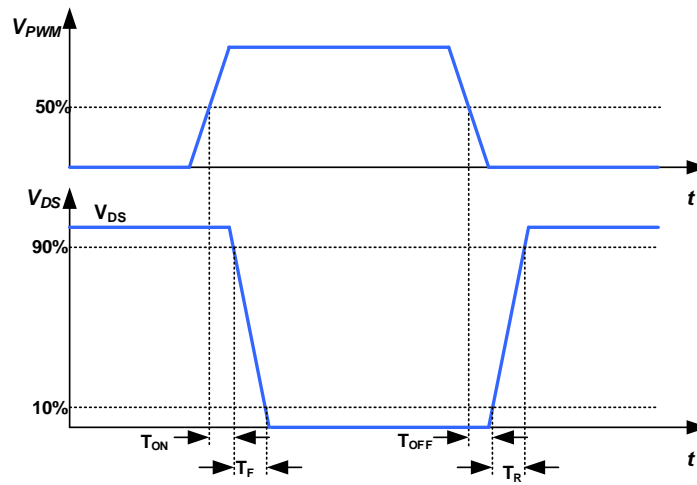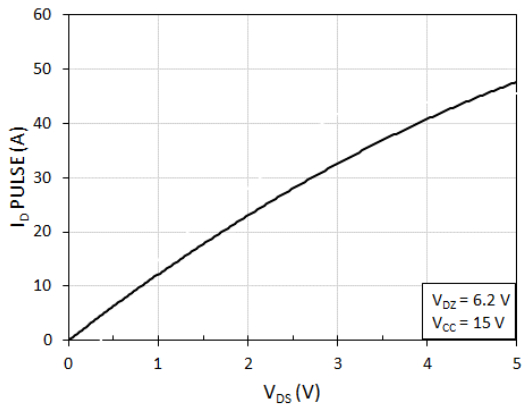


Fig. 1. Inductive switching circuit
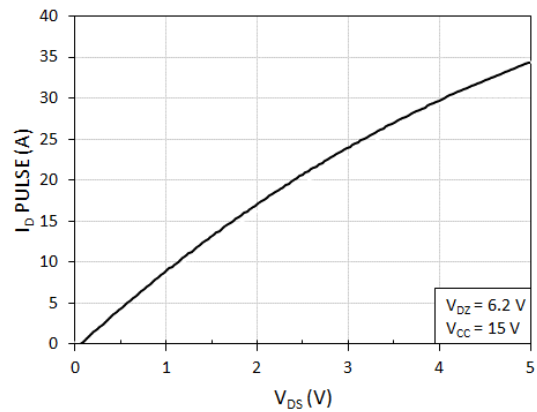


Fig. 2. Propagation delay and rise/fall time definitions
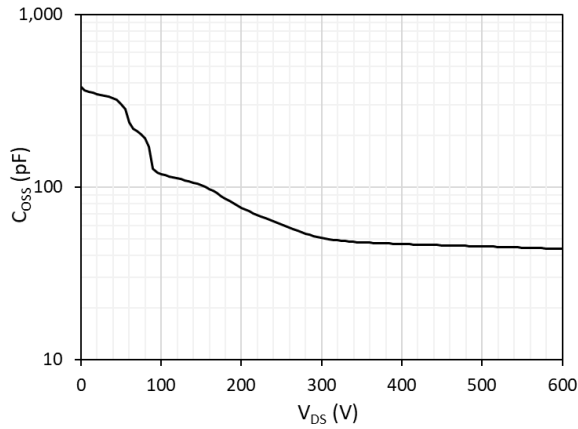
## Characteristic Graphs (Cont.)



Fig. 9. Output capacitance ($C_{OSS}$) vs. drain-to-source voltage ($V_{DS}$)
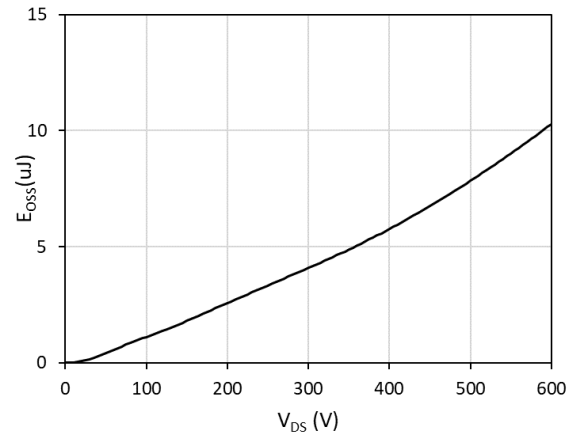


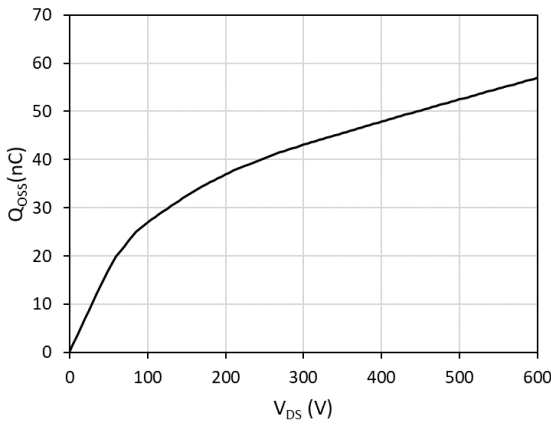Fig. 10. Energy stored in output capacitance ($E_{OSS}$) vs. drain-to-source voltage ($V_{DS}$)



Fig. 11. Charge stored in output capacitance ($Q_{OSS}$) vs. drain-to-source voltage ($V_{DS}$)
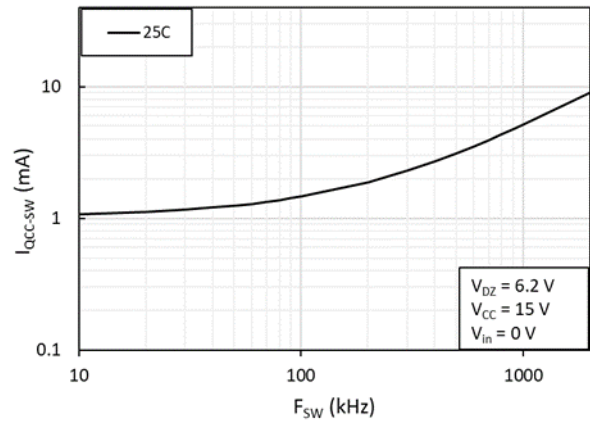


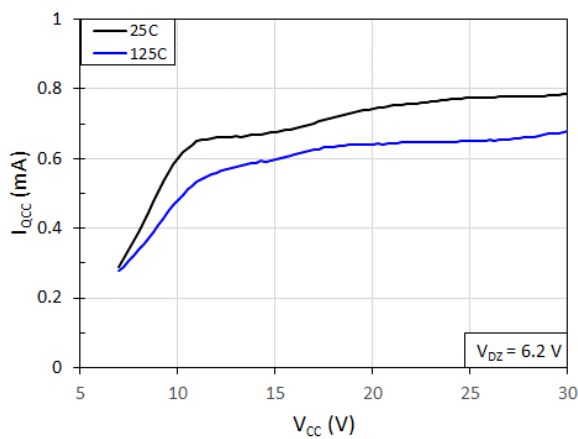Fig. 12. $V_{CC}$ operating current ($I_{QCC-SW}$) vs. operating frequency ($F_{SW}$)



Fig. 13. $V_{CC}$ quiescent current ($I_{QCC}$) vs. supply voltage ($V_{CC}$)
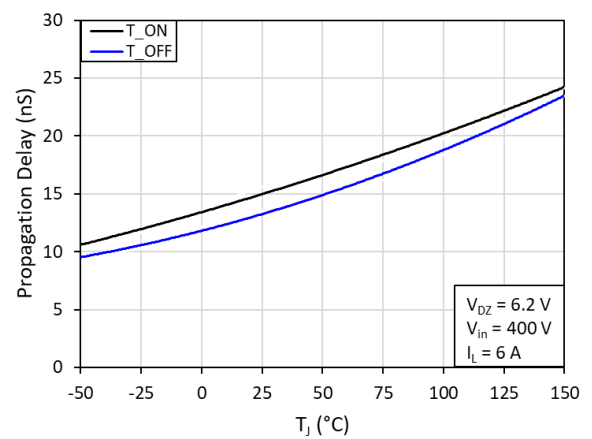


Fig. 14. Propagation delay ($T_{ON}$ and $T_{OFF}$) vs. junction temperature($T_J$)

## Characteristic Graphs (Cont.)



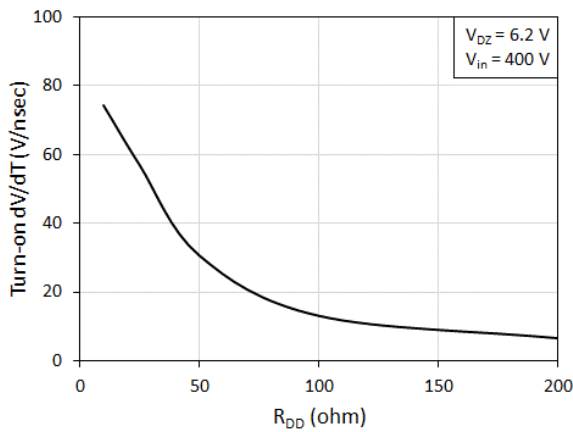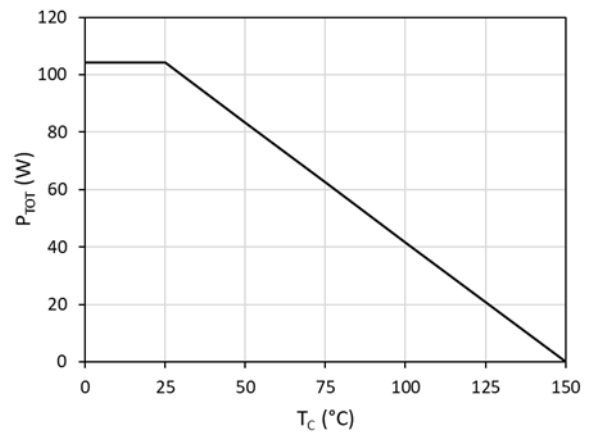Fig. 15. Slew rate (dV/dt) vs. gate drive turn-on current set resistance ($R_{DD}$) at T = 25 °C



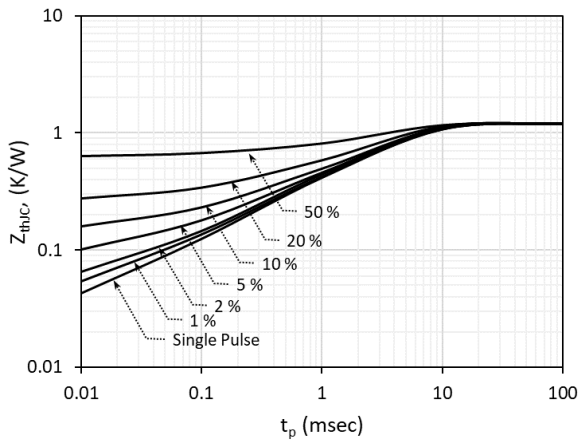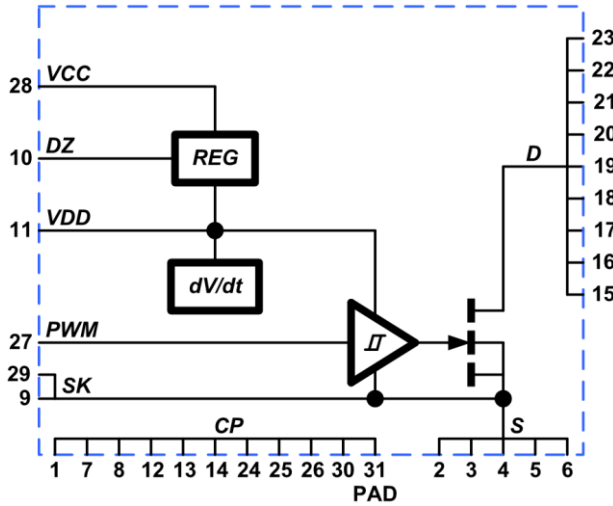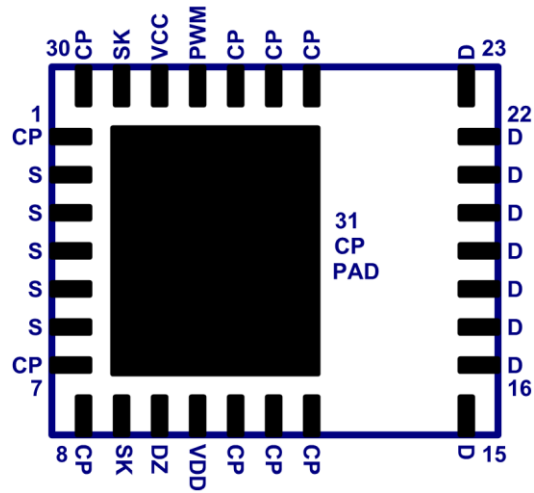Fig. 16. Power dissipation ($P_{TOT}$) vs. case temperature ($T_C$)



Fig. 17. Max. thermal transient impedance ($Z_{thJC}$) vs. pulse width ($t_P$)

## 7. Internal Schematic, Pin Configurations and Functions



Connect CP to S or PGND in PCB layout
See PCB layout section of this datasheet



Package Top View

| Pin | | I/O(1) | Description |
|---|---|---|---|
| **Number** | **Symbol** | | |
| 1,7,8,12,13,14,24,25,26,30,31 | CP | T | Metal cooling pad on bottom of package for thermal management. **CP must be connected to Source or circuit PGND. Do not leave CP unconnected or floating!** |
| 2,3,4,5,6 | S | O, G | Source of power FET & GaN IC supply ground. |
| 10 | $D_Z$ | I | Gate drive supply voltage set pin (connect 6.2 V Zener to GND). |
| 11 | $V_{DD}$ | I | Gate drive supply voltage. Gate drive turn-on current set pin (using $R_{DD}$). |
| 27 | PWM | I | PWM input |
| 28 | $V_{CC}$ | P | Supply voltage (10V to 24V) |
| 15,16,17,18,19,20,21,22,23 | D | P | Drain of power FET |
| 9, 29 | SK | SK | GaN IC Source Kelvin ground |

*(1) I = Input, O = Output, P = Power, G = GaN IC Ground, T = Thermal, SK = Source Kevin*

## 8. Functional Description

The following functional description contains additional information regarding the IC operating modes and pin functionality.

### 8.1. Start Up

When the $V_{CC}$ supply is first applied to the GaNFast power IC, care should be taken such that the $V_{DD}$ and $D_Z$ pins are up at their correct voltage levels before the PWM input signal starts. The $V_{DD}$ pin ramp up time is determined by the internal regulator current at this pin and the external $C_{VDD}$ capacitor. $C_{VDD}$ time constant should be calculated such that there is sufficient time to charge up the $C_{VDD}$ capacitor to ~6V. In some scenarios, where fast startup is required, an optional diode in parallel with the $R_{DD}$ can be used to ensure the $C_{VDD}$ capacitor is fully charged before the first PWM pulse is applied. Also, since the $D_Z$ pin voltage sets the $V_{DD}$ voltage level, the $V_{DD}$ pin will ramp up together with the $D_Z$ pin (Fig. 18).

For half-bridge configurations, it is important that the $V_{CC}$ supply, the $D_Z$ pin, and the $V_{DD}$ supply of the high-side GaNFast power IC are all charged up to their proper levels before the first high-side PWM pulses start. For LLC applications, a long on-time PWM pulse to the low-side (> 10 µs) is typically provided by the LLC controller to allow the supply pins of the high-side GaNFast power IC to charge up (through the external bootstrap diode) to their correct levels before the first high-side PWM pulses start (Fig. 19).
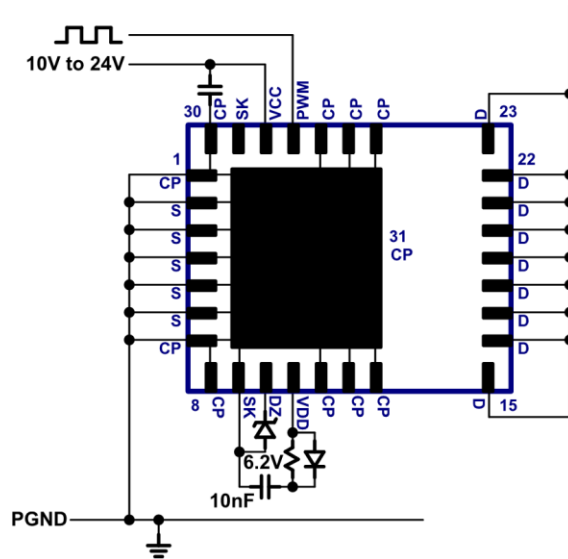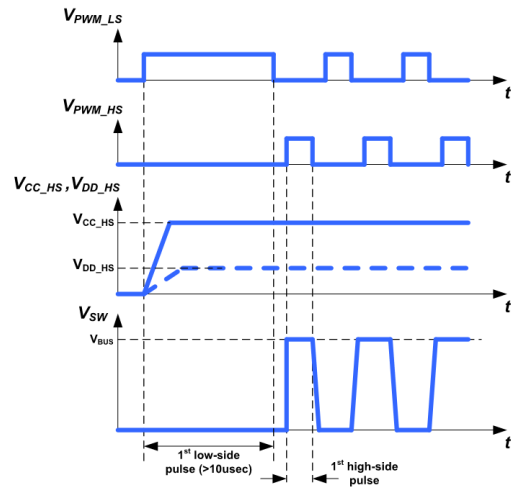


Fig. 18. Start-up circuit



Fig. 19. LLC half-bridge start-up timing diagram

## 8.2. Normal Operating Mode

During Normal Operating Mode, all of the internal circuit blocks are active. $V_{CC}$ is operating within the recommended range of 10 V to 24 V, the $V_{DD}$ pin is at the voltage set by the Zener diode at the $D_Z$ pin (6.2 V), and the internal gate drive and power FET are both enabled. The external PWM signal at the PWM pin determines the frequency and duty-cycle of the internal gate of the power FET. As the PWM voltage toggles above and below the rising and falling input thresholds (4 V and 1 V), the internal gate of the power FET toggles on and off between $V_{DD}$ and 0 V (Fig. 20). The drain of the power FET then toggles between the source voltage (typically power ground) and a higher voltage level (650 V max), depending on the external power conversion circuit topology.
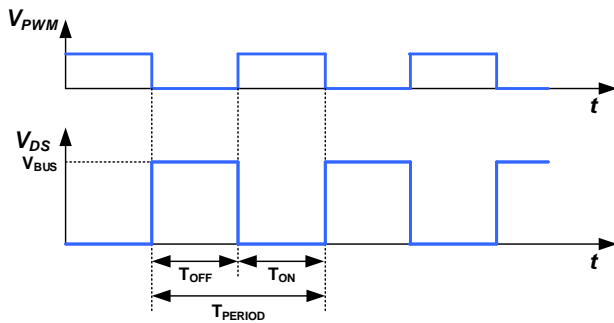


Fig. 20. Normal operating mode timing diagram

## 8.3. Programmable Turn-on dV/dt Control

During first start-up pulses or during hard-switching conditions, it is desirable to limit the slew rate (dV/dt) of the drain of the power FET during turn-on. This is necessary to reduce EMI or reduce circuit switching noise. To program the turn-on dV/dt rate of the internal power FET, a resistor ($R_{DD}$) is placed in between the $V_{DD}$ capacitor and the $V_{DD}$ pin. This resistor ($R_{DD}$) sets the turn-on current of the internal gate driver and therefore sets the turn-on falling edge dV/dt rate of the drain of the power FET (Fig. 21). A typical turn-on slew-rate change with respect to $R_{DD}$ is shown in Fig. 15. **Minimum 10 Ω $R_{DD}$ is required.**
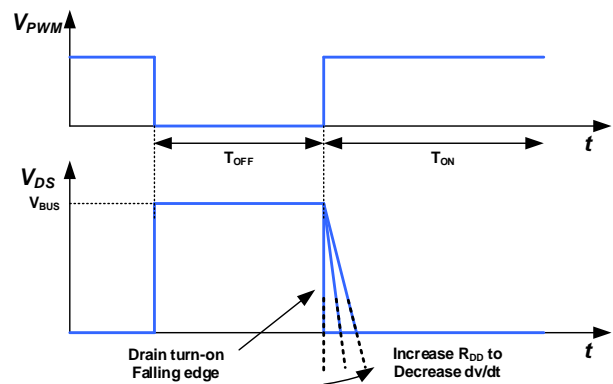


Fig. 21. Turn-on dV/dt slew rate control

## 8.4. Source Kelvin (SK) Ground Pins

For high current and hard-switching CCM applications, high-frequency switching noise due to PCB layout parasitic inductance should be minimized as much as possible. To further reduce high-frequency noise, this GaN Power IC includes two Source Kelvin (SK) pins (pin 9, pin 29). The SK pins are on-chip kelvin contacts to the Source and are separate from the high current Source connections (pins 2-7).The GND connections for components $C_{VDD}$ and $D_Z$ should be connected to SK pin 9, and the GND connection for $C_{VCC}$ should be connected to CP pin 30 (Fig. 22). SK pin 29 should be left unconnected (N/C). When using an external gate drive buffer for PWM, the GND of the external gate drive buffer should be connected to the SK pin 29. This will minimize any possible high frequency voltage spikes from occurring at the PWM input during switching.
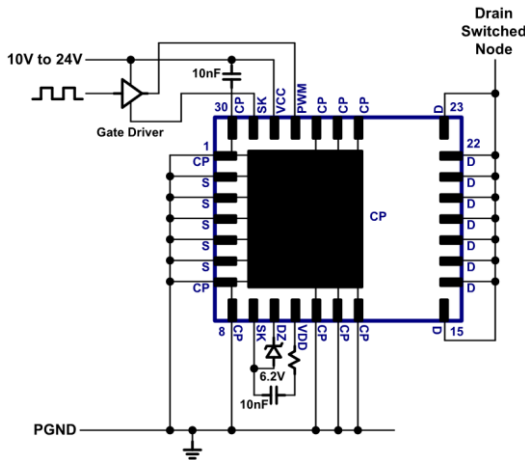
## 8.5. IC Footprint and Pin-to-Pin Compatibility

The NV6128 has the same footprint as other GaNFast ICs (i.e. NV6127) but pin-to-pin compatibility depends on the actual circuit configuration and if a current sensing resistor is used or not. The NV6128 is slightly different than the NV6127 due to the SK pins. For circuit configurations without an external current sensing resistor ($R_{CS}$) connected between the Source of the GaN IC and PGND, then placing the NV6128 onto the same PCB layout as the NV6127 will result in the SK pins of the NV6128 to be connected to CP and to Source. The NV6128 will function normally in this configuration and there is no need to change the PCB layout or GaN IC connections (Fig. 23). For circuit configurations with an external current sensing resistor connected between the Source of the GaN IC and PGND, the SK pins will be connected to CP and to the bottom of the $R_{CS}$ resistor, and the Source connections (pins 2-7) are connected at the top of the $R_{CS}$ resistor. This will result in large voltage spikes between SK and Source during switching transitions. In this case the SK pin connections will need to be disconnected from CP so a new PCB layout is necessary (Fig. 24). **Check the circuit configuration carefully and make sure SK, CP and Source pins are connected correctly!**
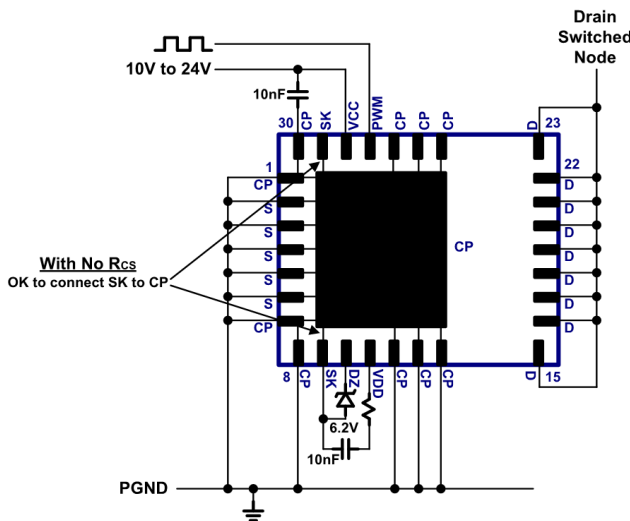


Fig. 22. SK pin connections



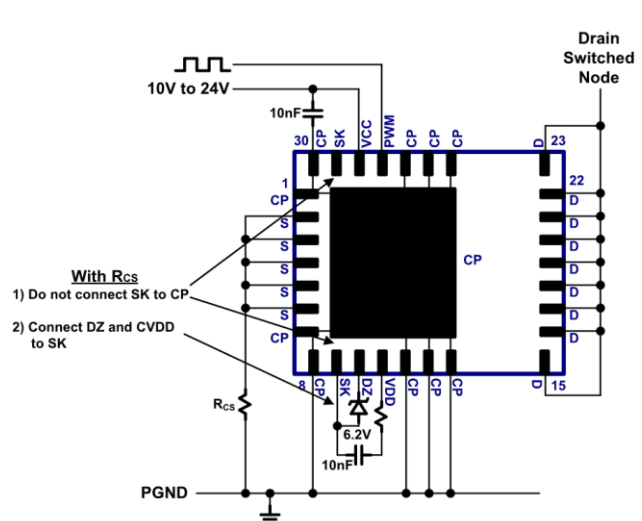Fig. 23 NV6128 with no $R_{CS}$ is compatible with NV6127 connections



Fig. 24 NV6128 with $R_{CS}$ is not directly compatible with NV6127 connections

## 8.6. Current Sensing

For many applications it is necessary to sense the cycle-by-cycle current flowing through the power FET. To sense the current flowing through the GaNFast power IC, a standard current-sensing resistor can be placed in between the source and power ground (Fig. 25). In this configuration, all of the components around the GaNFast power IC ($C_{VCC}$, $C_{VDD}$, $D_Z$, etc.) should be grounded with a single connection at the source. Also, an additional RC filter can be inserted between the PWM signal and the PWM pin (100 Ω, 100 pF typical). This filter is necessary to prevent false triggering due to high-frequency voltage spikes occurring at the source node due to external parasitic inductance from the source PCB trace or the current-sensing resistor itself. For increased cooling pad PCB copper area it may be desired to connect CP to the circuit PGND. Fig. 25 shows the components around the GaNFast power IC grounded at the source pins (S) and CP connected to PGND. This allows for all CP pins and CP pad to be connected to a large and continuous thermal copper area without being obstructed by the current sensing resistor. **CP cannot be float. CP must be connected to source (S) or circuit PGND!**
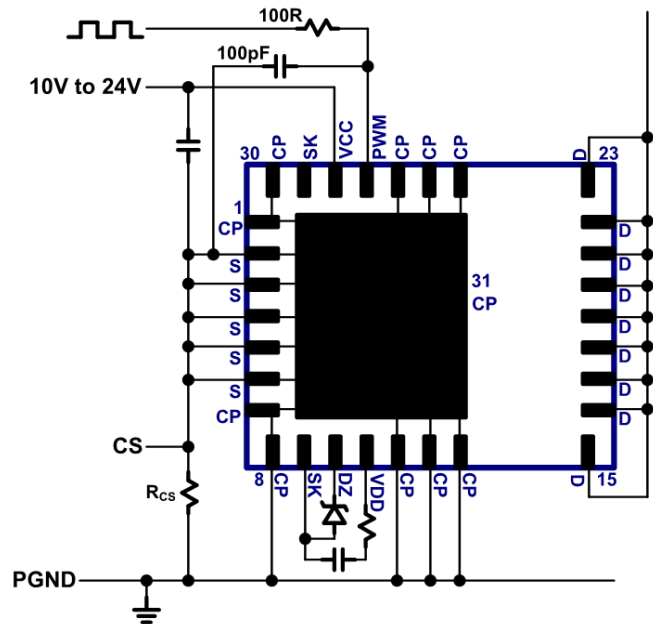


Fig. 25 Current sensing circuit

## 8.7. 3.3V PWM Input Circuit

For some applications where a 3.3 V PWM signal is required (DSP, MCU, etc.) an additional buffer can be placed before the PWM input pin (Fig. 26) with the buffer supply voltage connected to the $V_{DD}$ capacitor.
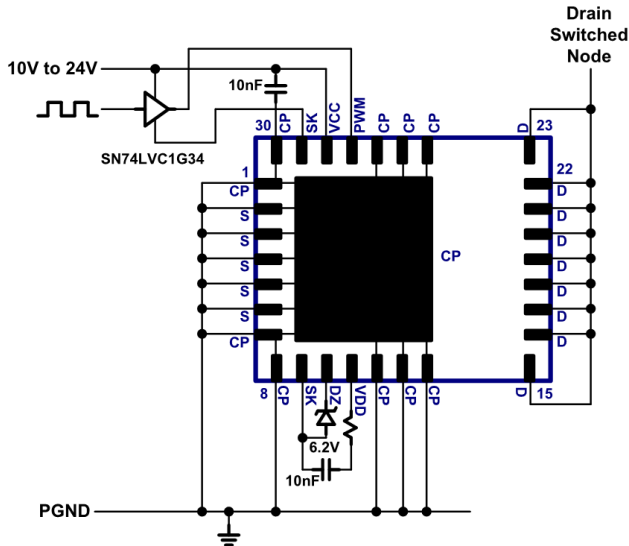


Fig. 26 3.3 V PWM input buffer circuit

## 8.8. PCB Layout Guidelines

The design of the PCB layout is critical for good noise immunity, sufficient thermal management, and proper operation of the IC. Typical PCB layout examples for without current sensing resistor and with current sensing resistor, are all shown in Section 10.

The following rules should be followed carefully during the design of the PCB layout:

1) Place all IC filter and programming components directly next to the IC. These components include ($C_{VCC}$, $C_{VDD}$, $R_{PWM}$, $C_{PWM}$, $R_{DD}$ and $D_Z$).

2) Keep ground trace of IC filter and programming components separate from power GND trace. Do not run power GND currents through ground trace of filter components!

3) For best thermal management, place thermal vias in the source pad area to conduct the heat out through the bottom of the package and through the PCB board to other layers (see Section 10 for correct layout examples).

4) Use large PCB thermal planes (connected with thermal vias to the source pad) and additional PCB layers to reduce IC temperatures as much as possible (see Section 10 for correct layout examples).

5) For half-bridge layouts, do not extend copper planes from one IC across the components or pads of the other IC!

6) For high density designs, use a 4-layer PCB and 2 oz. copper to route signal connections. This allows layout to maintain large thermal copper planes and reduce power device temperature.

## 8.9. Recommended Component Values

The following table (Table I) shows the recommended component values for the external filter capacitors, Zener diode, and $R_{DD}$ connected to the pins of the GaNFast power IC. These components should be placed as close as possible to the IC. Please see PCB Layout guidelines for more information. The Zener diode at the $D_Z$ pin should be a low-current type with a flat knee, and the min/max limits must be followed. $R_{DD}$ must be a minimum of 10 Ω to ensure application and device robustness.

| SYM | DESCRIPTION | PART NO. | SUPPLIER | MIN | TYP | UNITS |
|---|---|---|---|---|---|---|
| $C_{VCC}$ | Maximum $V_{CC}$ supply capacitor | | | | 10 | nF |
| $C_{VDD}$ | $V_{DD}$ supply capacitor | | | 47 | | nF |
| $R_{DD}$ | Gate drive turn-on current set resistor | | | 10 | 25 | Ω |
| $D_Z$ | $V_{DD}$ set Zener diode ($D_Z$ pin) | BZT52B6V2 RHG | Taiwan Semiconductor Corporation | 5.8 | 6.2 | V |
| | | MM3Z6V2ST1G | ON-Semiconductor | | | |
| | | PDZ6.2B.115 | Nexperia (NXP) | | | |
| | | PLVA662A.215 | Nexperia (NXP) | | | |
| | | LM3Z6V2T1 | Leshan Radio Company | | | |
| $R_{PWM}$ | PWM filter resistor | | | | 100 | Ω |
| $C_{PWM}$ | PWM filter capacitor | | | | 100 | pF |

Table I. Recommended component values.

## 8.9.1. Zener Diode Selection

The Zener voltage is a critical parameter that sets the internal reference for gate drive voltage and other circuitry. The Zener diode needs to be selected such that the voltage on the $D_Z$ pin is within recommended operating conditions (5.8 V to 6.6 V) across operating temperature (-40°C to 125°C) and bias current (10 µA to 1 mA). To ensure effective operation, the current vs. voltage characteristics of the Zener diode should be measured down to 10 µA to ensure flat characteristics across the current operating range (10 µA to 1 mA). The recommended part numbers (Table I) meet these requirements. If the Zener selected by user does not ensure that the voltage on the $D_Z$ pin is always within the recommended operating range, the functionality and reliability of the GaNFast power IC can be impacted.

## 8.10. Drain-to-Source Voltage Considerations

GaN Power ICs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies, such as quasi-resonant (QR) flyback applications. The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Fig. 27. When the device is switched off, the energy stored in the transformer leakage inductance will cause $V_{DS}$ to overshoot to the level of $V_{SPIKE}$. The clamp circuit should be designed to control the magnitude of $V_{SPIKE}$. It is recommended to apply an 80% derating from $V_{DS\ (TRAN)}$ rating (800V) to 650 V max for repetitive $V_{DS}$ spikes under the worst case steady-state operating conditions. After dissipation of the leakage energy, the device $V_{DS}$ will settle to the level of the bus voltage plus the reflected output voltage which is defined in Fig. 27 as $V_{PLATEAU}$. It is recommended to design the system such that $V_{PLATEAU}$ follows a typical derating of 80% (520V) from $V_{DS\ (CONT)}$ (650V). Finally, $V_{DS\ (TRAN)}$ (800V) rating is also provided for events that occur on a non-repetitive basis, such as line surge, lightning strikes, start-up, over-current, short-circuit, load transient, and output voltage transition. 800V $V_{DS(TRAN)}$ ensures excellent device robustness and no-derating is needed for these non-repetitive events, assuming the surge duration is < 100 µs. For half-bridge based topologies, such as LLC, $V_{DS}$ voltage is clamped to the bus voltage. $V_{DS}$ should be designed such that it meets the $V_{PLATEAU}$ derating guideline (520V).
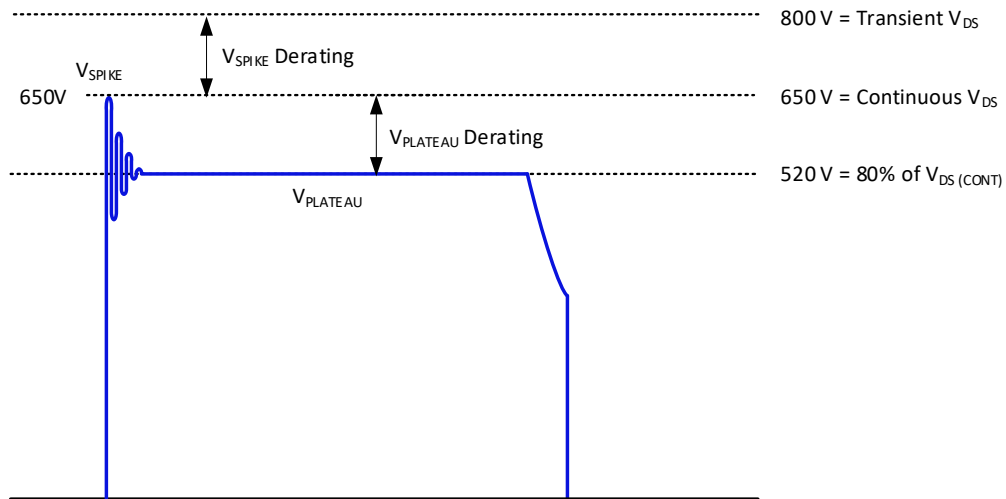


Fig. 27 QR flyback drain-to-source voltage stress diagram

## 9. Recommended PCB Land Pattern
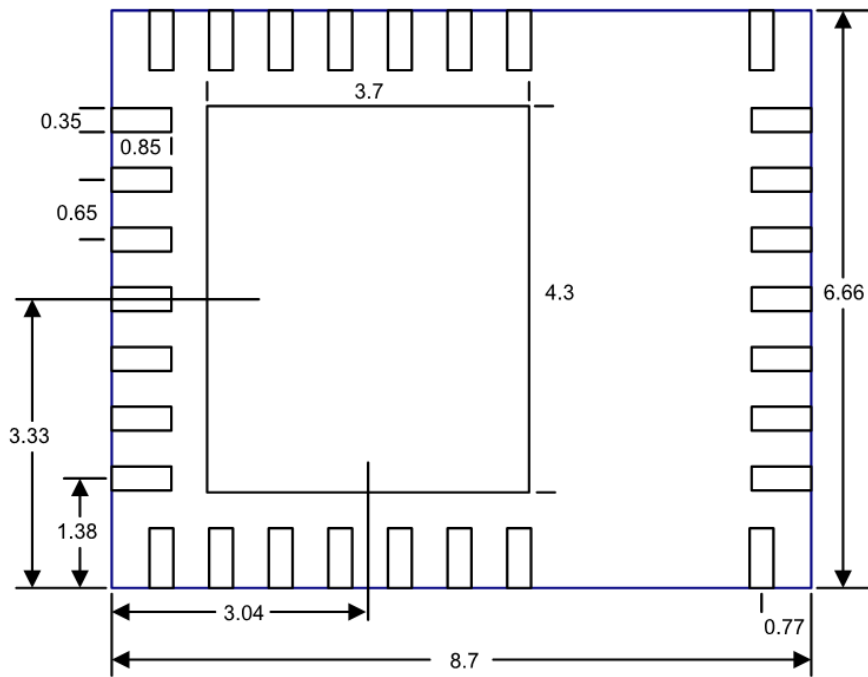


All dimensions are in mm
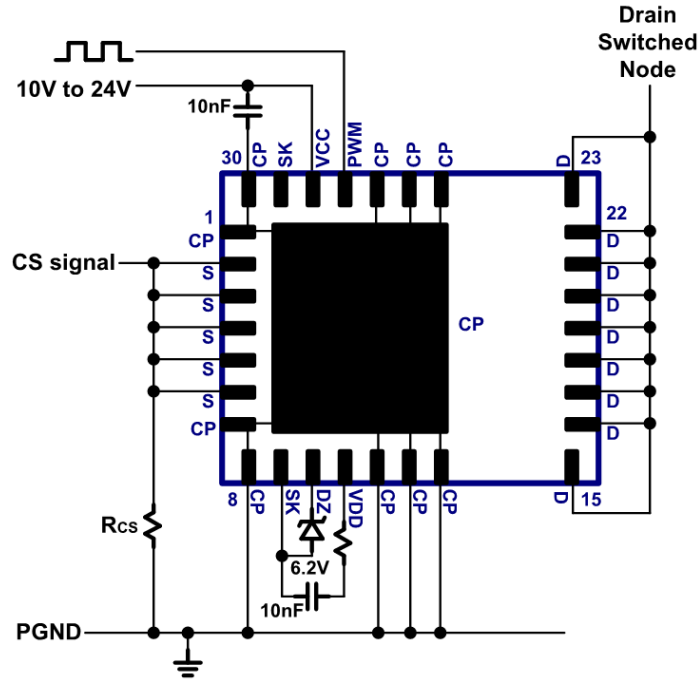
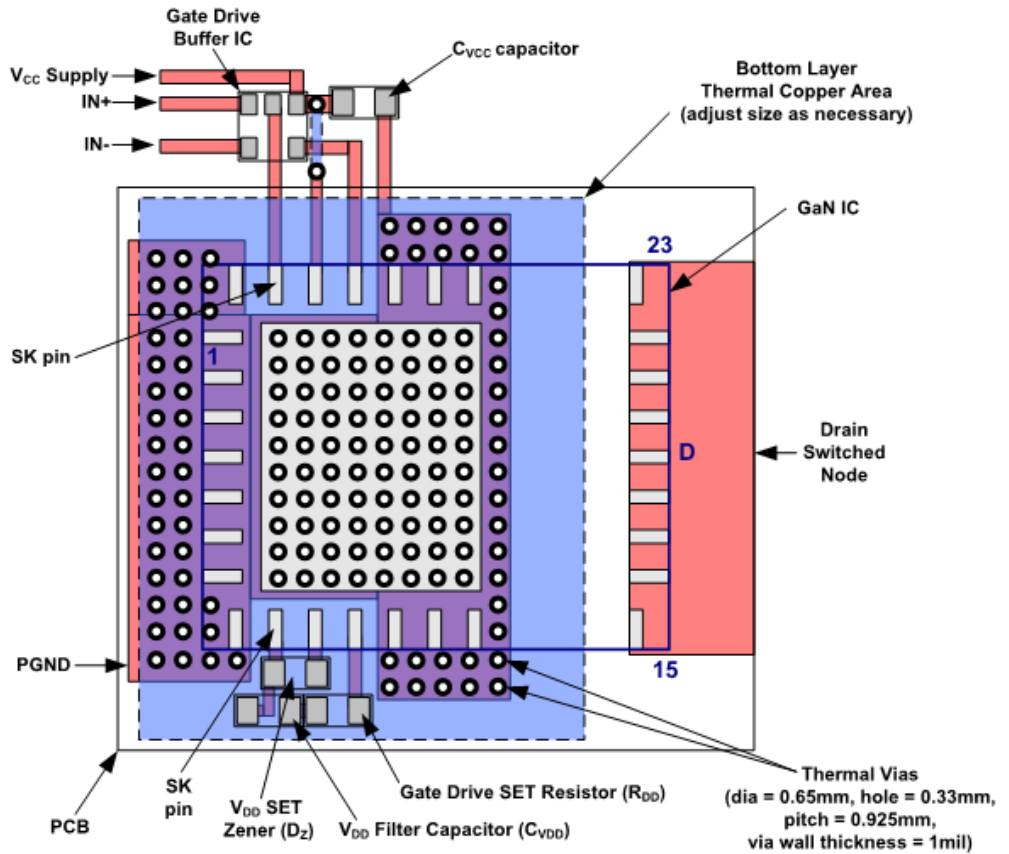## 10. PCB Layout Guidelines

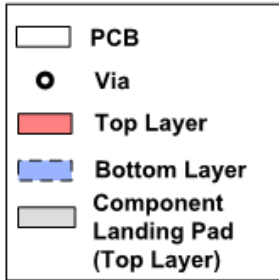**Without CS Resistor:**
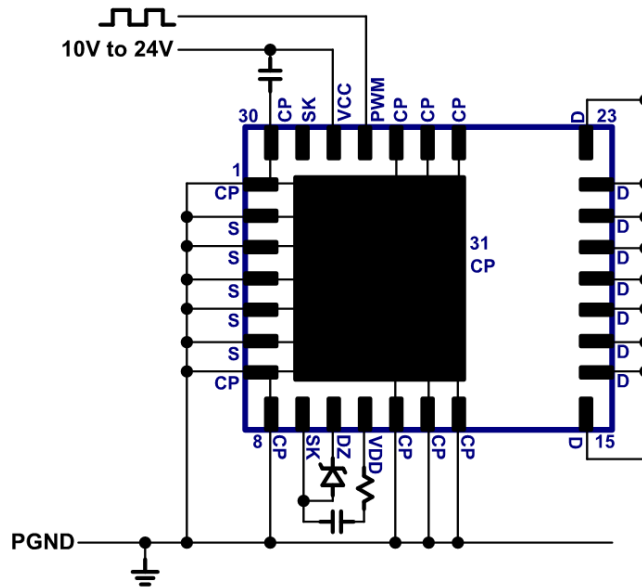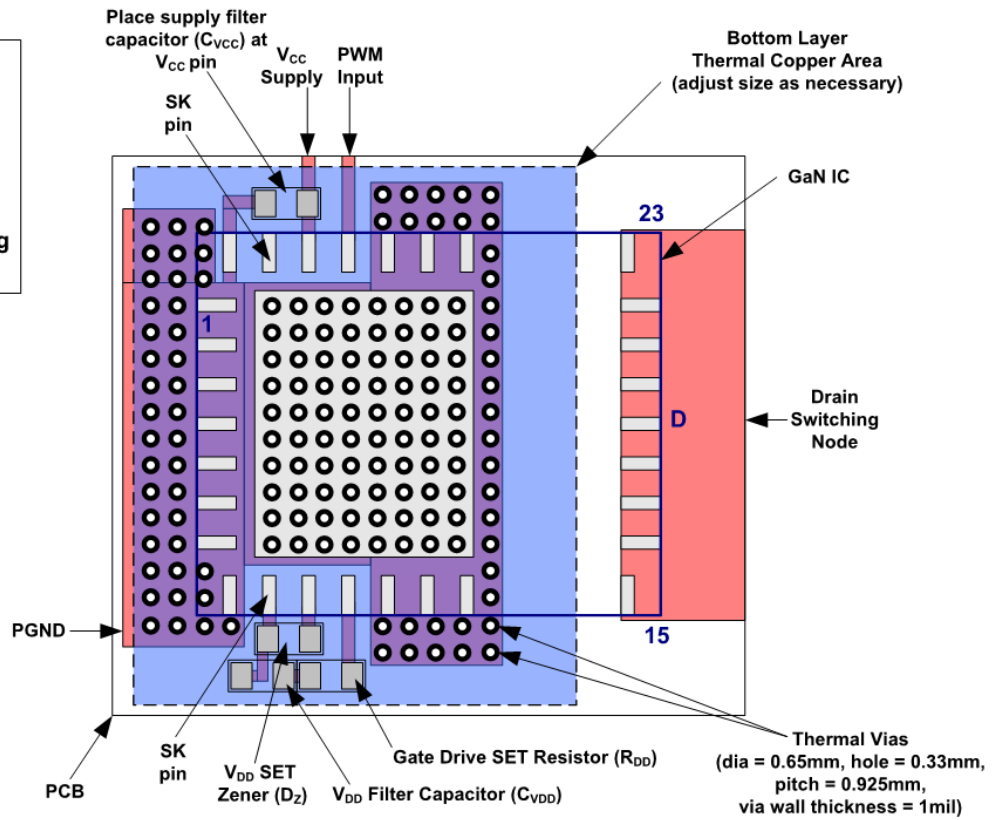




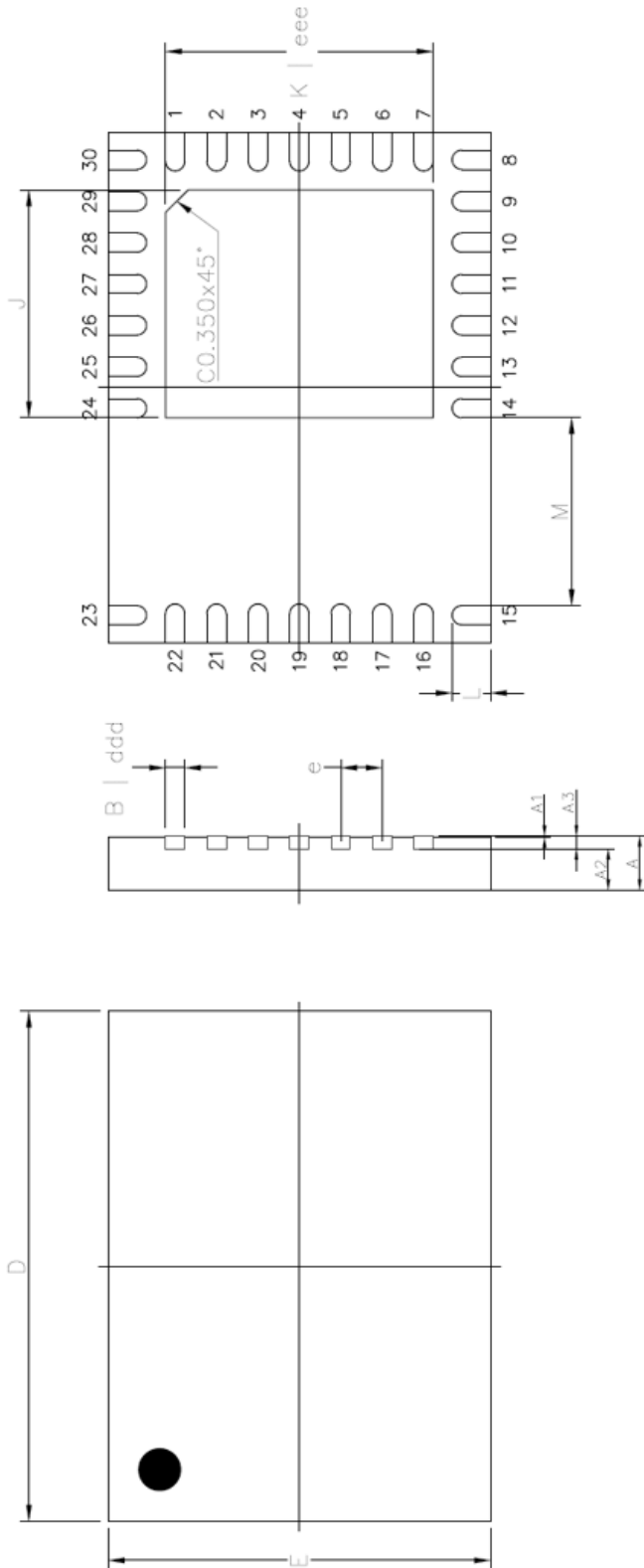(Top View)

**With CS Resistor:**
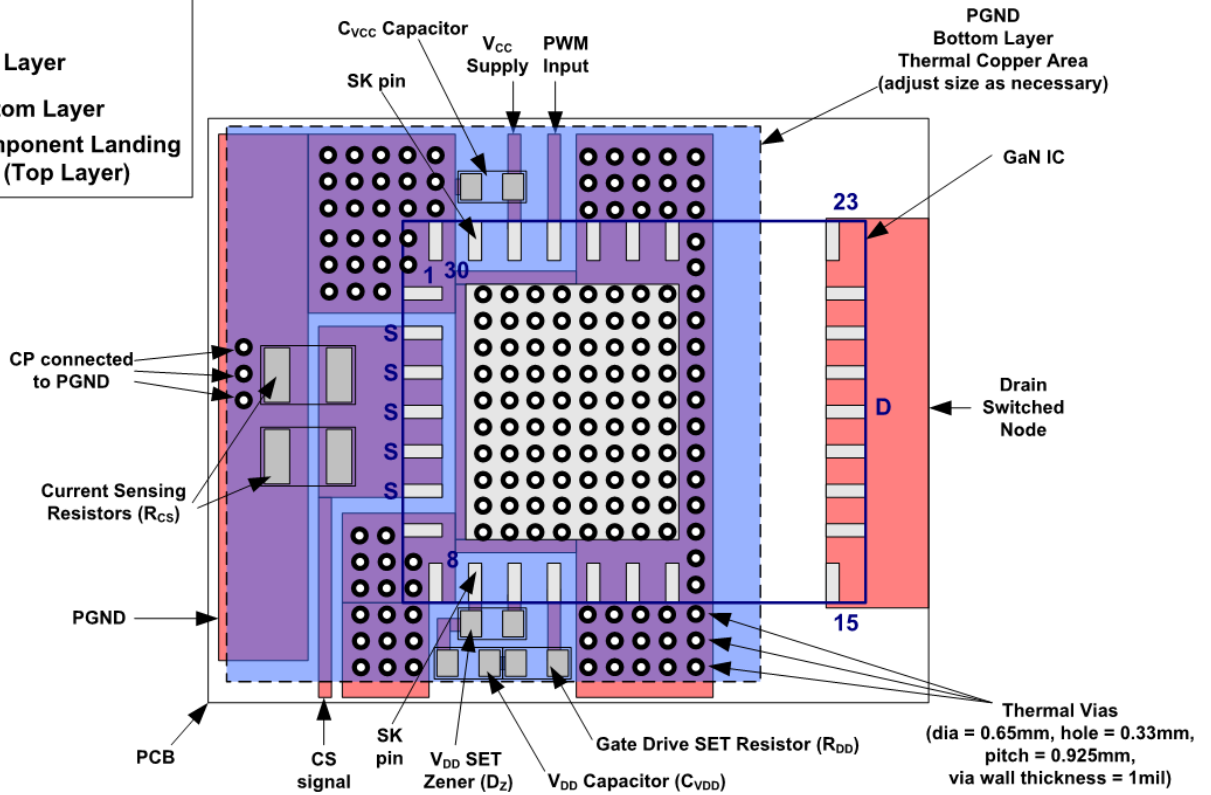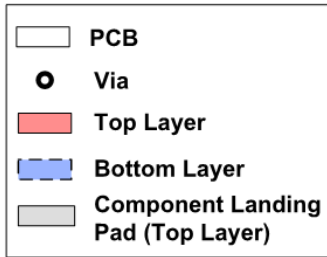




**(Top View)**

**With Gate Driver Buffer (no R$_{CS}$):**
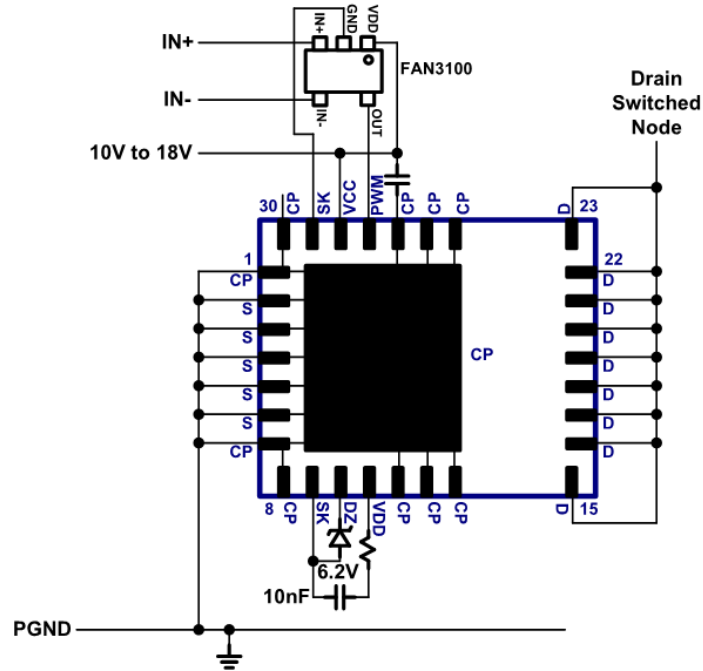


(Top View)

## 11. QFN Package Outline



| SYMBOL | | MIN | NOM | MAX | |
|---|---|---|---|---|---|
| TOTAL THICKNESS | A | 0.8 | 0.85 | 0.9 | |
| STAND OFF | A1 | 0 | 0.02 | 0.05 | |
| MOLD THICKNESS | A2 | --- | 0.65 | --- | |
| L/F THICKNESS | A3 | | 0.203 REF | | |
| LEAD WIDTH | B | 0.4 | 0.45 | 0.5 | |
| BODY SIZE | D | | 8 BSC | | |
| | E | | 6 BSC | | |
| LEAD PITCH | e | | 0.65 BSC | | |

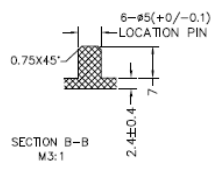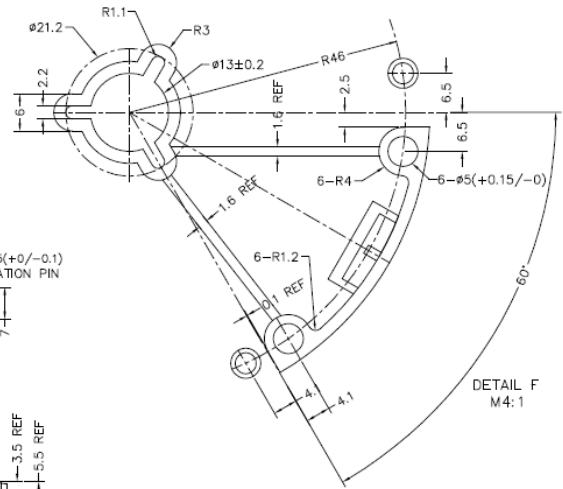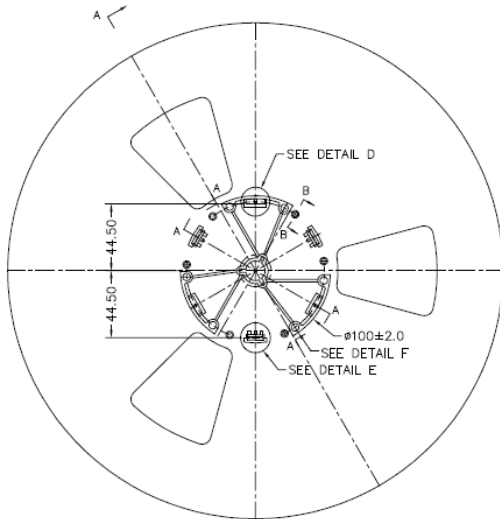| SYMBOL | | MIN | NOM | MAX |
|---|---|---|---|---|
| EP SIZE | X | 3.475 | 3.575 | 3.675 |
| | Y | 4.1 | 4.2 | 4.3 |
| LEAD LENGTH | L | 0.625 | 0.675 | 0.725 |
| HIGH VOLTAGE SPACING | M | 2.85 | 2.95 | 3.05 |
| PACKAGE EDGE TOLERANCE | aaa | | 0.1 | |
| MOLD FLATNESS | bbb | | 0.1 | |
| COPLANARITY | ccc | | 0.08 | |
| LEAD OFFSET | ddd | | 0.1 | |
| EXPOSED PAD OFFSET | eee | | 0.1 | |

## 12. Tape and Reel Dimensions



SECTION A – A
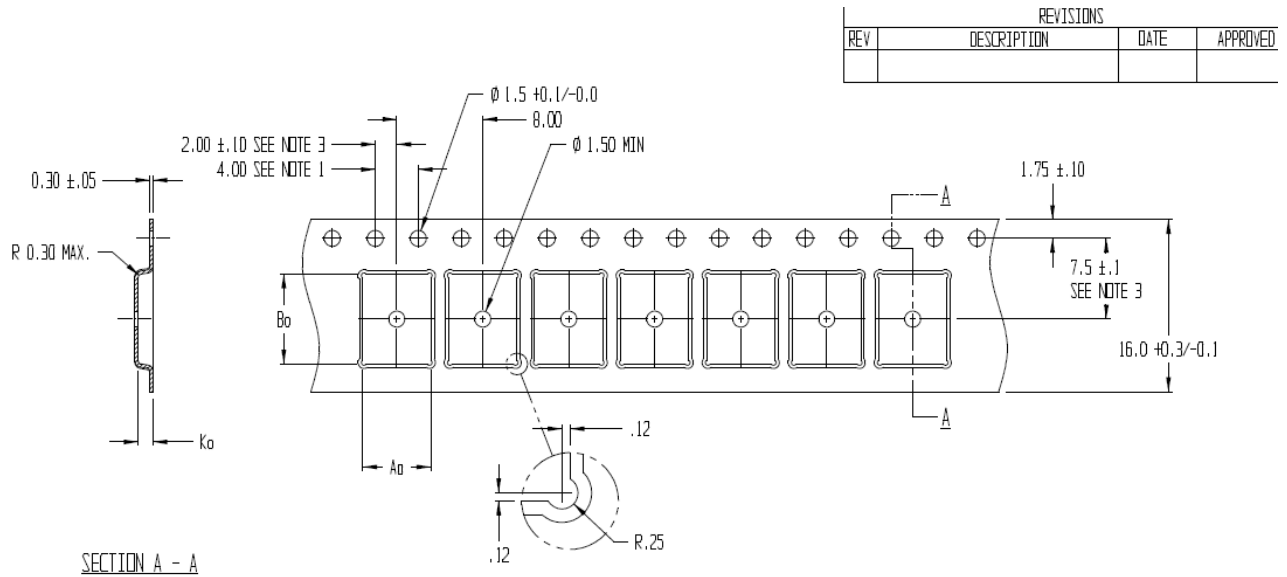
Ao = 6.35
Bo = 8.35
Ko = 1.40

7" Reel
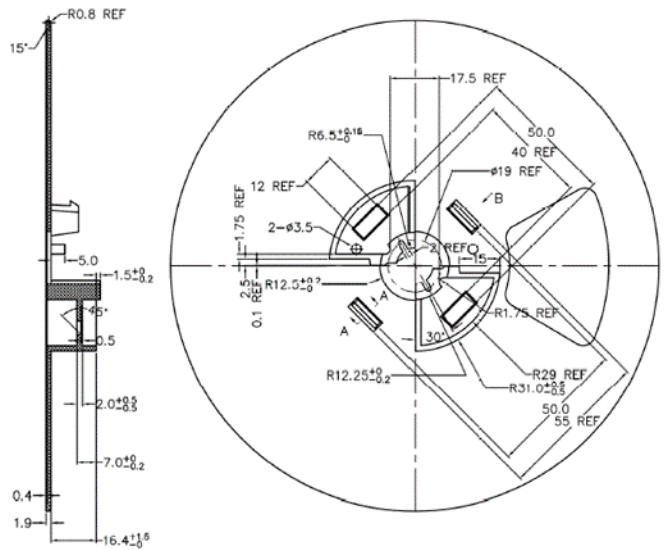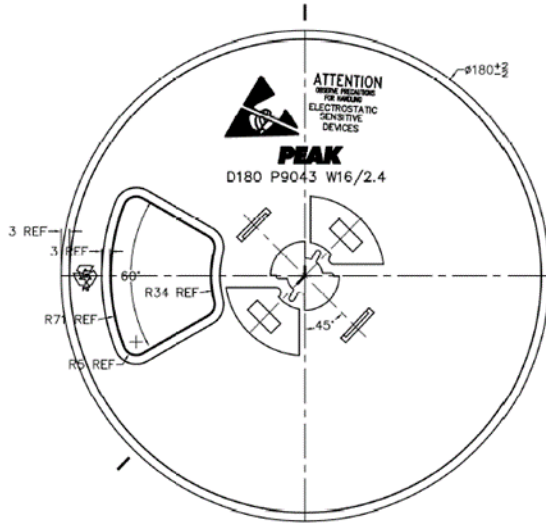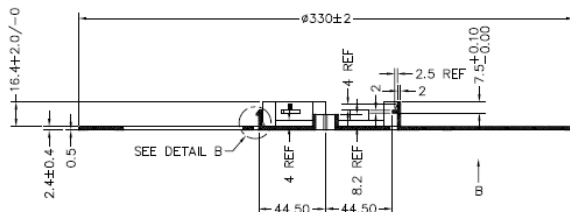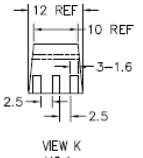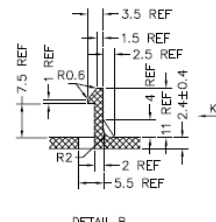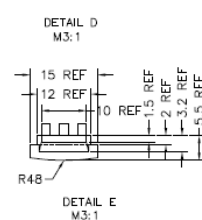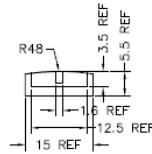


13" Reel

## 13. Ordering Information

| Part Number | Operating Temperature Grade | Storage Temperature Range | Package | MSL Rating | Packing (Tape & Reel) |
|---|---|---|---|---|---|
| NV6128 | -40 °C to +125 °C $T_{CASE}$ | -55 °C to +150 °C $T_{CASE}$ | 6 x 8 mm QFN | 3 | 5,000 : 13" Reel |
| NV6128-RA | -40 °C to +125 °C TCASE | -55 °C to +150 °C TCASE | 6 x 8 mm QFN | 3 | 1,000 : 7" Reel |

## 14. Revision History

| Date | Status | Notes |
|---|---|---|
| Dec 16, 2020 | Initial Release | First publication |

## Additional Information

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